EXPRESS MAIL NO. EV 398572652 US Attorney Docket No: N1085-00180 [TSMC2003-0325]

REMARKS/ARGUMENTS

Claims 1-31 are pending in this application with claims 3, 4, 28 and 29 having been previously withdrawn from consideration. Claims 1, 2, 5-27, 30 and 31 are rejected.

In this paper, claims 1 and 27 are being amended. Applicants respectfully request re-examination, reconsideration and allowance of claims 1-2, 5-27 and 30-31.

I. Claim Rejections - 35 U.S.C. §102

On page 3, first line of the subject Office action, claims 1-2, 5-7, 9-15, 18-27 and 30 were rejected under 35 U.S.C. §102(a) or (e) as being anticipated by Mathew et al (U.S. 2003/0151077), hereinafter "Mathew". Applicants respectfully submit that these claim rejections are overcome for reasons set forth below.

Independent **Claim 30** recites the features of:

> etching portions of said gate electrode material not covered by said patterned masking layer to produce a gate electrode that traverses said semiconductor fin; and
>
> with said patterned masking layer in place, introducing dopant impurities into said semiconductor fin to form source and drain active regions therein.

The Office action states, on page 4, penultimate paragraph, "With respect to Claim 30, Mathews discloses the use of a masking layer to form source and drain regions. See paragraph 24, page 2." Mathew does not, however, disclose using the same patterned masking layer used to form a gate electrode, to form source and drain active regions in the semiconductor fin. Moreover, Mathew does not teach the introduction of dopant impurities into the semiconductor fin with the patterned masking layer in place: rather; the photoresist step in paragraph 24 of Mathew is "used to pattern the polysilicon layer 28 to expose current electrodes in the form of source/drain regions . . . The source/drain regions 52, 54 are extensions of the fin region 24 that will subsequently be doped to form the source and drain regions of a transistor." This

masking step is clearly not used as an implant mask during the step in which dopant impurities are introduced into the semiconductor fin to form source/drain regions as Mathew concedes, in ¶ [0024] that the source/drain regions are not yet doped after using this photoresist mask.

Claim 30 is distinguished from Mathew and therefore the rejection of claim 30, should be withdrawn.

Independent **Claim 1** has been amended. Amended independent claim 1 recites the features of:

> said gate electrode material having a top surface; and
>
> planarizing said top surface to form a planarized top surface that extends directly over said semiconductor fin.

This feature of the top surface of the gate electrode material being directly over the semiconductor fin distinguishes the present invention from Mathew which does not teach this feature of a planarized top surface of a gate electrode extending over the semiconductor fin. Claim 1 and therefore also dependent claims 2 and 5-26 are distinguished from Mathew and therefore the rejection of claims 1, 2, 5-7, 9-15 and 18-26 under 35 U.S.C. §102 as being anticipated by Mathew, should be withdrawn.

Amended independent **Claim 27** also recites the features that appear in claim 1 and are reproduced above. Claim 27 is therefore distinguished form Mathew and the rejection of claim 27 under 35 U.S.C. §102, should be withdrawn. Independent claim 27 further recites the features:

> forming spacers on sides of said gate electrode; and
>
> performing selective epitaxy on exposed portions of said semiconductor fin but not on said spacers thereby increasing height and width of said semiconductor fin.

Mathew does not teach forming spacers on the side of the gate electrodes then epitaxially growing a film on the semiconductor fin while using the spacers to prevent

growth of the epitaxially film in certain portions on sides of the gate electrode. On page 4, fourth paragraph (referencing claims 9-11), the Office action states that "Mathew et al. disclose spacers and patterning and implanting. See Figure 15, and page 2, paragraph 22." Applicants respectfully point out that Fig. 15 includes no features described as spacers in the corresponding specification section and that paragraph 22 does not teach spacers. Applicants thereby would appreciate further clarification regarding the grounds of this rejection.

It appears that the only "spacer" reference in Mathew is found in paragraphs 27 and 31 and the spacers identified in paragraphs 27 and 31 do not satisfy the limitations of the claimed spacers. The "spacer" etch in paragraph 27 refers to a method for separating electrodes formed on opposed sides of the semiconductor fin ("The spacer etch is performed in lieu of a CMP process") and these 2 electrodes do not appear to be used to spatially direct any growth or other physical processes. With respect to paragraph 31, nitride spacers are formed prior to a silicidation process and not to provide spatial selectivity to an epitaxial growth process performed to increase the width and height of the semiconductor fin in the source/drain regions, as in the claimed invention. Claim 27 is therefore further distinguished from Mathew. As above, the rejection of claim 27 under 35 U.S.C. § 102, should be withdrawn.

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CONCLUSION

Based on the foregoing, each of pending claims 1-2, 5-27 and 30-31 is in allowable form and the application in condition for allowance, which action is respectfully and expeditiously requested.

The Assistant Commissioner for Patents is hereby authorized to charge any fees or credit any excess payment that may be associated with this communication to Deposit Account 04-1679.

Respectfully submitted,

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